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PATENT
0465-0552P 183

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPELLANT: SONG, Chi Hyung

SERIAL NO.: 09/241,413 EXAMINER: Kostak, V.

FILED: February 2, 1999 GROUP: 2611

FOR: DEVICE FOR CONVERTING VIDEO FORMAT

APPEAL BRIEF

Assistant Commissioner of Patents
Washington, D.C. 20231

February 15, 2001

Sir:

Appellant submits herewith a Brief on Appeal in triplicate as required by 37 C.F.R. 1.192. This Brief on Appeal responds to the Final Office Action dated August 18, 2000 and the Advisory Action dated December 1, 2000.

I. REAL PARTY IN INTEREST

The real party in interest is LG ELECTRONICS INC., a corporation of Korea.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant which will directly affect or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS:

Claims 4-9 and 11-31 remain pending in this application. These claims are reproduced in the attached Appendix.

Claims 4, 24-27, 29, and 31 stand finally rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Donovan (U.S. Patent No. 5,914,753) [1]. Claims 17-23 and 30 are allowed. Claims 5-9 [2], 11-16, and 28 would be allowable if rewritten in independent form.

The Section 102 rejection above is being appealed.

IV. STATUS OF AMENDMENTS:

An Amendment After Final under Rule 116 was filed on November 20, 2000, containing proposed changes to claims 8 and 15. The Advisory Action dated November 15, 2000 stated that the Amendment After Final will be entered upon the filing of this Brief. Accordingly, the changes to claims 8 and 15 are reflected in the Appendix.

V. SUMMARY OF THE INVENTION:

The present invention relates to an improved device for converting one video format to another video format. An embodiment of the invention illustrated in Fig. 3A includes a vertical format converting unit 200 and a horizontal format converting unit 300, each of which includes a

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[1] Despite the Examiner's continuing mention of the Horii and Gray references (Final Office Action, page 4, section 3; and Advisory Action, section 4), Donovan is the only reference used as a basis for a § 102 or § 103 rejection.

[2] Claims 5-7 were not listed in the Advisory Action, but were indicated as being allowable in the Final Office Action.

processing unit 32 and a control unit 31, shown, for example, in Fig. 3B (specification, page 7, lines 4-15). The control unit 31 provides an equation, for converting an input format to an output format, to the first and second processing units 32A and 32B in the processing unit 32 (specification, page 7, lines 11-21; Fig. 3C). As shown in Figs. 5 and 7, each of the processing units 32A and 32B includes a numerator generating unit 323 and a denominator generating unit 324 for respectively generating a numerator and a denominator in the respective video conversion equation (specification, page 10, lines 3-16). In this manner, the vertical format converting unit 200 and the horizontal format converting unit 300 in Fig. 3A respectively convert the format of their data according to an equation, having a numerator and a denominator, which is determined from the input and desired output data formats.

VI. ISSUES PRESENTED FOR REVIEW:

A. Whether a *prima facie* case of anticipation under 35 U.S.C. § 102 has been established by the Examiner for any of claims 4, 24-27, 29, and 31.

B. Whether Donovan teaches all the elements of claim 31, as is required for a proper rejection under 35 U.S.C. § 102(e).

C. Whether Donovan teaches all the elements of claim 29, as is required for a proper rejection under 35 U.S.C. § 102(e).

D. Whether Donovan teaches all the elements of claims 4 and 24-27, as is required for a proper rejection under 35 U.S.C. § 102(e).

VII. GROUPING OF CLAIMS:

Claims 4, 24-27, 29, and 31 do not stand or fall together. Independent claim 29 stands or falls alone. Independent claim 31 stands or falls alone. Claims 4 and 24-27 stand or fall together.

VIII. ARGUMENT:

A. A *prima facie* case of anticipation has not been established for any of claims 4, 24-27, 29, and 31.

1. "Shorthand" rejections are improper for newly added claims.

After the first Office Action dated May 1, 2000, Appellant canceled claims 1-3, and added new claims 24-27, 29, and 31. However, instead of addressing each element of the newly added claims 24-27, 29, and 31, the Examiner stated, without further elaboration, in the Final Office Action "[t]he rejections in the previous Office action therefore apply to the redrafted claims 24-27, 29, and 31." The elements of, e.g., new independent claims 24, 29, and 31 differ from the elements of, e.g., canceled claim 1. In using such a shorthand reference to a rejection of canceled claims 1-3, the Examiner ignores, refuses to address, and otherwise reads out of the claims all different elements in the newly presented claims. Because this shorthand rejection did not address all claim elements, a *prima facie* case of anticipation has not been established for claims 24-27, 29, and 31 [3]. The § 102(e) rejection of all claims should be reversed on this ground.

2. The new claims have not been read with particularity on Donovan.

Even if such "shorthand" rejections were proper for newly presented claims, the Examiner has not read, e.g., independent claims 24, 29, or 31 with particularity on Donovan. 37 C.F.R.

§ 104(c)(2) requires of the Examiner that "the particular part [of the reference] relied on must be designated as nearly as practicable." However, none of the elements in these new independent claims were read on particular components (e.g., 206, 208, or 212 cited in the first Office Action) in Donovan, forcing Appellant to guess at the components which the Examiner considers to anticipate the elements of new claims 24-27, 29, and 31. The rejection of these claims in the Final Office Action is neither "complete" nor "totally proper" as alleged in the Advisory Action, and at most amounts to an unsupported allegation of anticipation. Such an allegation cannot establish a *prima facie* case, and the § 102(e) rejection of all claims should be reversed on this additional ground.

B. Donovan fails to teach all the elements of claim 31.

Appellant respectfully traverses the rejection of claim 31 over Donovan. Claim 31 requires a device including, *inter alia*, "a controller ... determining a conversion equation from the determined input video format and the determined desired output video format."[4] Donovan does not teach the claimed device. The SRC controller 208 in Fig. 15 of Donovan merely passes a mode (0-6) to the scan rate converter 206 (col. 10, lines 15-18). The scan rate converter 206 in turn determines television signal parameters by performing a lookup in the parameter table 224 (col. 10, lines 17-31). Neither the controller 208 nor the scan rate converter 206 "determin[es] a conversion equation from the determined input video format and the determined desired output video format," as set forth in claim 31. Nor has the Examiner identified a component in the portions (col. 3, lines 27-30;

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[3] And claim 4 by virtue of its dependence from claim 26.

[4] This quote from claim 31 contradicts the Examiner's assertion on page 2 of the Final Office Action that "the claim simply recites determining an input format and a desired output format."

and col. 9, lines 7-22) of Donovan cited in the Final Office Action which determines a conversion equation, as set forth in claim 31. Because Donovan fails to teach all elements of the claim, the rejection of claim 31 is improper and should be reversed.

C. Donovan fails to teach all the elements of claim 29.

Appellant respectfully traverses the rejection of claim 29 over Donovan. Claim 29 requires a device including, *inter alia*, "a horizontal format converting unit . . . including, a second operation unit for being configured to perform an arithmetic operation, and a second control unit determining a horizontal conversion operation to convert the output of the vertical format converting unit into a desired horizontal format based on the determined converting mode, and configuring the operation unit to perform the horizontal conversion operation." Donovan does not teach the claimed device.

On page 3 of the Final Office Action, the Examiner cites "the clock circuit of Donovan" as allegedly corresponding to the claimed second operation unit, but provides no element number or other proof of such allegation from Donovan. The Examiner then implies the existence of a clock controller, because "[the clock circuit] is clearly under some control rather than functioning arbitrarily." The Examiner apparently deduces the existence of "a clock circuit" and "a clock controller" based on a remark by Appellant on page 18 of the Amendment dated July 31, 2000, stating that in Donovan "horizontal format conversion is obtained through control of the clock signal" (see Final Office Action, page 3, lines 1-5 generally, and lines 4 and 5 particularly).

However, Appellant's acknowledgement of a clock signal in Donovan does not imply some deduced clock circuit and clock controller having the attributes of the second operation unit and

second control unit set forth in claim 29. Rather, Donovan teaches only that the scan rate converter 206 in Fig. 15 determines various television signal parameters by performing a lookup into the parameter table 224 (col. 10, lines 15-20). Among the parameters stored by the parameter table 224 are various line memory write and read clock values (col. 10, lines 23-26 and Table 2). Hence, Appellant's remark in the Amendment referred only to a clock signal produced by the scan rate converter 206 and the parameter table 224 taught in Donovan.

Neither of the scan rate converter 206 and the parameter table 224 is "configured to perform an arithmetic operation," as required by the second operation unit set forth in claim 29. Also, neither component of Donovan "determin[es] a horizontal conversion operation to convert the output of the vertical format converting unit into a desired horizontal format based on the determined converting mode," as required by the second control unit set forth in claim 29. Because Donovan fails to teach all elements of the claim, the rejection of claim 29 is improper and should be reversed.

D. Donovan fails to teach all the elements of claims 4 and 24-27.

Appellant respectfully traverses the rejection of claims 4 and 24-27 over Donovan. Claims 4 and 24-27 each require a device including, *inter alia*, "a numerator generating unit...configuring to calculate the numerator portion of the conversion equation in response to the control signals; and a denominator generating unit...configuring to divide the output of the numerator generating unit by the denominator portion in response to the control signals." Donovan does not teach the claimed device. Rather than point to specific components of Donovan, on page 3 of the Final Office Action,

the Examiner cites "text from col. 11, line 23." From col. 11, line 12 to col. 14, line 35 of Donovan, there is presented a mathematical discussion of how to compute various VGA and television parameters (col. 14, lines 6-10). There is no teaching in this cited section of Donovan of the claimed numerator generating unit and denominator generating unit. Further, television signal parameters (e.g., in col. 10, Table 2) stored in a parameter table 206 in Fig. 15 of Donovan also do not teach the claimed numerator generating unit and denominator generating unit. Because Donovan also fails to teach all elements of claims 4 and 24-27, the rejection of these claims is improper and should be reversed.

IX. CONCLUSION

For the reasons set forth above, each of the rejections in the Final Office Action dated August 18, 2000 is improper. It is therefore respectfully requested that the Examiner be reversed on all grounds.

Respectfully submitted,

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X. APPENDIX

4. A device as claimed in claim 26, wherein the operand mapping unit comprises;

a first multiplexer for providing one of the present luminance signal and the previous luminance signal as a first value 'a' to the numerator generating unit, and

a second multiplexer for providing one of the present luminance signal and the previous luminance signal as a second value 'b' to the numerator generating unit.

5. A device as claimed in claim 4, wherein the numerator generating unit comprises:

a first shift left for shifting the first value 'a' from the first multiplexer to a left direction by units of an (n)th power of 2 (2^n, n = 0, 1, 2, ---), to provide a plurality of values (a, 2a, 4a, 8a, ---) from the first value 'a', which are first intermediate operands,

a second shift left for shifting the second value 'b' from the second multiplexer to a left direction by units of an (n)th power of 2 (2^n, n = 0, 1, 2, ---), to provide a plurality of values(b, 2b, 4b, 8b, ---) from the second value 'b', which are second intermediate operands, and

an operation processing unit for conducting operations required for obtaining final operands and the numerator portion in the conversion equation from the first intermediate operands and the second intermediate operands.

6. A device as claimed in claim 5, wherein the operation processing unit comprises:

a third multiplexer for receiving the values a, 2a, 4a, 8a from the first shift left and selecting and forwarding one of the values under the control of the controller,

a fourth multiplexer for selectively providing either one of "a" and "0" from the first shift left under the control of the controller,

a fifth multiplexer for selectively providing either one of values b, 2b, 4b, and 8b from the second shift left under the control of the controller,

a sixth multiplexer for receiving the values 4b, 8b, and 16b from the second shift left and "0" and selectively providing any one of the received ones under the control of the controller,

a seventh multiplexer for receiving the values b, 2b, and 4b from the second shift left and "0" and selectively providing any one of the received ones under the control of the controller,

an operator for selectively subjecting a value from the third multiplexer and a value from the fourth multiplexer to a different operation,

a first adder for adding values from the fifth multiplexer and the first multiplexer,

a subtracter for subtracting a value from the seventh multiplexer from a value from the first adder, and

a second adder for adding values from the operator and the subtracter, to generate a numerator portion fl of the conversion equation.

7. A device as claimed in claim 6, wherein the operator is either an adder or a subtracter.

8. A device as claimed in claim 24, wherein the denominator generating unit comprises:

a shift right shifting the numerator portion fl from the numerator generating unit by units of (n)th power (n=0, 1, 2, 3, ---) of 2 in a right direction, to provide a plurality of values 2, 1/4, 1/8, 1/16, --- (n=0, 1, 2, 3, ---), and

an operation processing unit for processing operations required for obtaining denominator portion of the conversion equation and a luminance signal having a final converted format using the plurality of values.

9. A device as claimed in claim 8, wherein the operation processing unit comprises:

an eighth multiplexer for receiving the values fl, fl/2, and fl/4 from the shift right and providing one of the values under the control of the controller,

a first divider for dividing a value from the eighth multiplexer by three,

a ninth multiplexer for selectively providing either one of a value fl from the numerator generating unit and the value from the first divider,

a second divider for dividing a value from the ninth multiplexer by "five",

a third divider for dividing a value from the first divider by "three", and

a tenth multiplexer for selectively providing one of values from the first, second, and third dividers, the present luminance signal, and a value from the shift right as a converted luminance signal under the control of the controller.

11. A device as claimed in claim 28, wherein the operand mapping unit comprises:

a third multiplexer for providing one of the present luminance signal and the previous luminance signal as a first initial operand value 'a' to the numerator generating unit, and

a fourth multiplexer for providing one of the present luminance signal and the previous luminance signal as a second initial operand value 'b' to the numerator generating unit.

12. A device as claimed in claim 11, wherein the numerator generating unit comprises:

a first shift left for shifting the value 'a' from the third multiplexer to a left direction by units of an (n)th power of 2 (2^n, n = 0, 1, 2, ---), to provide a plurality of values (a, 2a, 4a, 8a, ---) from the value 'a', which are first intermediate operands,

a second shift left for shifting the value 'b' from the fourth multiplexer to a left direction by units of an (n)th power of 2 (2^n, n = 0, 1, 2, ---), to provide a plurality of values (b, 2b, 4b, 8b, ---) from the value 'b', which are second intermediate operands, and

an operation processing unit for conducting operations required for obtaining final operands and the numerator portion in the conversion equation from the first intermediate operands and the second intermediate operands.

13. A device as claimed in claim 12, wherein the operation processing unit comprises:

a third multiplexer for receiving the values a, 2a, 4a, 8a from the first shift left and selecting and forwarding one of the values under the control of the controller,

a fourth multiplexer for selectively providing either one of "a" and "0" from the first shift left under the control of the controller,

a fifth multiplexer for selectively providing either one of values b, 2b, 4b, and 8b from the second shift left under the control of the controller,

a sixth multiplexer for receiving the values 4b, 8b, and 16b from the second shift left and "0" and selectively providing any one of the received ones under the control of the controller,

a seventh multiplexer for receiving the values b, 2b, and 4b from the second shift left and "0" and selectively providing any one of the received ones under the control of the controller,

an operator for selectively subjecting a value from the third multiplexer and a value from the fourth multiplexer to a different operation,

a first adder for adding values from the fifth multiplexer and the first multiplexer,

a subtracter for subtracting a value from the seventh multiplexer from a value from the first adder, and

a second adder for adding values from the operator and the subtracter, to generate a numerator portion f1 of the conversion equation.

14. A device as claimed in claim 13, wherein the operator is either an adder or a subtracter.

15. A device as claimed in claim 28, wherein the denominator generating unit comprises:

a shift right shifting the numerator portion f1 from the numerator generating unit by units of (n)th power (n=0, 1, 2, 3, ---) of 2 in a right direction, to provide a plurality of values 2, 1/4, 1/8, 1/16, --- (n=0, 1, 2, 3, ---), and

an operation processing unit for processing operations required for obtaining denominator portion of the conversion equation and a luminance signal having a final converted format using the plurality of values.

16. A device as claimed in claim 15, wherein the operation processing unit comprises

an eighth multiplexer for receiving the values f1, f1/2, and f1/4 from the shift right and providing one of the values under the control of the controller,

a first divider for dividing a value from the eighth multiplexer by three,

a ninth multiplexer for selectively providing either one of a value f1 from the numerator generating unit and the value from the first divider,

a second divider for dividing a value from the ninth multiplexer by "five",

a third divider for dividing a value from the first divider by "three", and

a tenth multiplexer for selectively providing one of values from the first, second, and third dividers, a present chrominance signal, and a value from the shift right as a converted chrominance signal under the control of the controller.

17. A digital television receiver, comprising:

an antenna;

a tuner for synchronizing to a desired channel signal;

an intermediate frequency signal generating unit for generating an intermediate frequency signal of the synchronized channel signal;

an audio signal processing unit for processing an audio signal only in the intermediate frequency signal so that the audio signal is audible;

a video signal processing unit for processing a video signal only in the intermediate frequency signal for obtaining chrominance signals and a luminance signal;

a filter unit for low pass filtering the video signal from the video signal processing unit;

a vertical format converting unit for converting a video signal format from the filter unit in a vertical direction to match to a desired output signal format; and,

a horizontal format converting unit for converting a video signal format from the vertical format converting unit in a horizontal direction to match to a desired output video signal format, wherein each of the vertical format converting unit and the horizontal format converting unit includes;

a control unit for determining an operation conducted at the present time, recognizing an operation to be conducted at the next time based on the operation conducted at the present time, and providing control signals suitable for the operation to be conducted at the next time, according to an input video format of an input video signal and an output video format of an output video signal desired to provide,

a first processing unit for converting a luminance signal format in the input video signal into a desired output video format,

a second processing unit for converting a chrominance signal format in the input video signal into a desired output video format, and

a separating unit for separating the received video signal into chrominance signals and a luminance signal.

18. A device as claimed in claim 17, wherein the first processing unit includes;

a delay for delaying a received luminance signal,

an operand mapping unit for utilizing the delayed luminance signal from the delay and a luminance signal received presently in determining initial operands to be used in a conversion operation equation, i.e., a first value 'a' and a second value 'b', according to a format conversion ratio,

a numerator generating unit for generating a numerator in the conversion operation equation using the operands of the conversion operation equation from the operand mapping unit, and

a denominator generating unit for selecting a denominator of the conversion operation equation, dividing the numerator of the conversion operation equation from the numerator generating unit with the selected denominator, to obtain a converted luminance signal.

19. A device as claimed in claim 18, wherein the operand mapping unit includes;

a first multiplexer for providing a first value 'a', an initial operand, of the conversion operation equation according to a format conversion using the delayed luminance signal Y1 from the delay and a luminance signal Y2 received presently, and

a second multiplexer for providing a second value 'b', an initial operand, of the conversion operation equation according to a format conversion using the delayed luminance signal Y1 from the delay and a luminance signal Y2 received presently.

20. A device as claimed in claim 18, wherein the numerator generating unit includes;

a first shift left for shifting the first value 'a' from the first multiplexer to a left direction by units of an (n)th power of 2 (2^n, n = 0, 1, 2, ---), to provide a plurality of values(a, 2a, 4a, 8a, ---) from the first value 'a', which are first intermediate operands,

a second shift left for shifting the second value 'b' from the second multiplexer to a left direction by units of an (n)th power of 2 (2^n, n = 0, 1, 2, ---), to provide a plurality of values(b, 2b, 4b, 8b, ---) from the second value 'b', which are second intermediate operands, and

an operation processing unit for conducting operations required for obtaining the final operands and the numerators in the conversion operation equation from the first intermediate operands and the second intermediate operands.

21. A device as claimed in claim 18, wherein the denominator generating unit shifts the numerator fl from the numerator generating unit by units of (n)th power (n=0, 1, 2, 3, ---) of 2 in a right direction, to provide a plurality of values ½, 1/4, 1/8, 1/16, --- (n=0, 1, 2, 3, ---), and

an operation processing unit for processing operations required for obtaining denominator of the conversion operation equation and a luminance signal having a final converted format using the plurality of values.

22. A device as claimed in claim 17, wherein the second processing unit includes;

a delay for delaying a chrominance signal,

an averaging unit for averaging a chrominance signal Cn-1 received presently and the chrominance signal delayed in the delay,

a first multiplexer for selectively providing either one of the chrominance signal received presently and a value from the averaging unit under the control of the control unit, and

a second multiplexer for selectively providing either one of the chrominance signal Cn delayed in the delay and a value from the averaging unit under the control of the control unit,

an operand mapping unit for utilizing the delayed luminance signal from the delay and a luminance signal received presently in determining initial operands to be used in a conversion operation equation, i.e., a first value 'a' and a second value 'b', according to a format conversion ratio,

a numerator generating unit for generating a numerator in the conversion operation equation using the operands of the conversion operation equation from the operand mapping unit, and

a denominator generating unit for selecting a denominator of the conversion operation equation, dividing the numerator of the conversion operation equation from the numerator generating unit with the selected denominator, to obtain a converted luminance signal.

23. A device as claimed in claim 17, further comprising a ratio detecting unit for detecting a format conversion ratio from an input video format to an output video format and providing the detected format conversion ratio to the vertical format converting unit and the horizontal format converting unit.

24. A device for converting a video format, comprising:

a controller determining a conversion equation to convert a video signal into a desired format based on a conversion mode, the conversion equation have a numerator portion and a denominator portion, and outputting control signals based on the determined conversion equation;

a numerator generating unit receiving at least one of a present video signal and a previous video signal, configuring to calculate the numerator portion of the conversion equation in response to the control signals, and calculating the numerator portion using the received at least one of present and previous signals; and

a denominator generating unit receiving output of the numerator generating unit, configuring to divide the output of the numerator generating unit by the denominator portion in response to the control signals, and dividing the output of the numerator generating unit by the denominator portion to obtain output video signal of the desired format.

25. The device as claimed in claim 24, wherein the present and previous video signals are luminance signals.

26. The device as claimed in claim 24, further comprising:

an operand mapping unit receiving the present luminance signal and the previous luminance signal, and selectively supplying the present luminance signal and the previous luminance signal to components of the numerator generating unit.

27. The device as claimed in claim 24, wherein the present and previous video signals are chrominance signals.

28. The device as claimed in claim 26, further comprising:

an averaging unit averaging the present chrominance signal and the previous chrominance signal to obtain and averaged chrominance signal;

a first multiplexer selectively outputting one of the averaged chrominance signal and the present chrominance signal;

a second multiplexer selectively outputting one of the averaged chrominance signal and the previous chrominance signal; and

an operand mapping unit receiving output from the first and second multiplexers, and selectively supplying the output from the first and second multiplexers to components of the denominator generating unit.

29. A device for converting a video format, comprising:

a vertical format converting unit receiving a video signal and determining a converting mode, and including,

a first operation unit for being configured to perform an arithmetic operation, and

a first control unit determining a vertical conversion operation to convert the video signal into a desired vertical format based on the determined converting mode, and configuring the operation unit to perform the vertical conversion operation; and

a horizontal format converting unit receiving output of the vertical format converting unit, and including,

a second operation unit for being configured to perform an arithmetic operation, and

a second control unit determining a horizontal conversion operation to convert the output of the vertical format converting unit into a desired horizontal format based on the determined converting mode, and configuring the operation unit to perform the horizontal conversion operation.

30. A device for converting a video format, comprising

a control unit determining an operation to convert an input video signal into a video signal of desired format, the determined operation including at least one of a multiplication operation and a division operation; and

a processing unit performing the determined operation based on control signals from the control unit, the processing unit performing the at least one of the multiplication operation and the division operation by shifting in a shifter a value to be one of multiplied and divided.

31. A device for converting a video format, comprising:

a controller determining an input video format, determining a desired output video format and determining a conversion equation from the determined input video format and the determined desired output video format; and

a processing unit converting input video signals from the determined input video format to the determined desired output video format using the conversion equation.